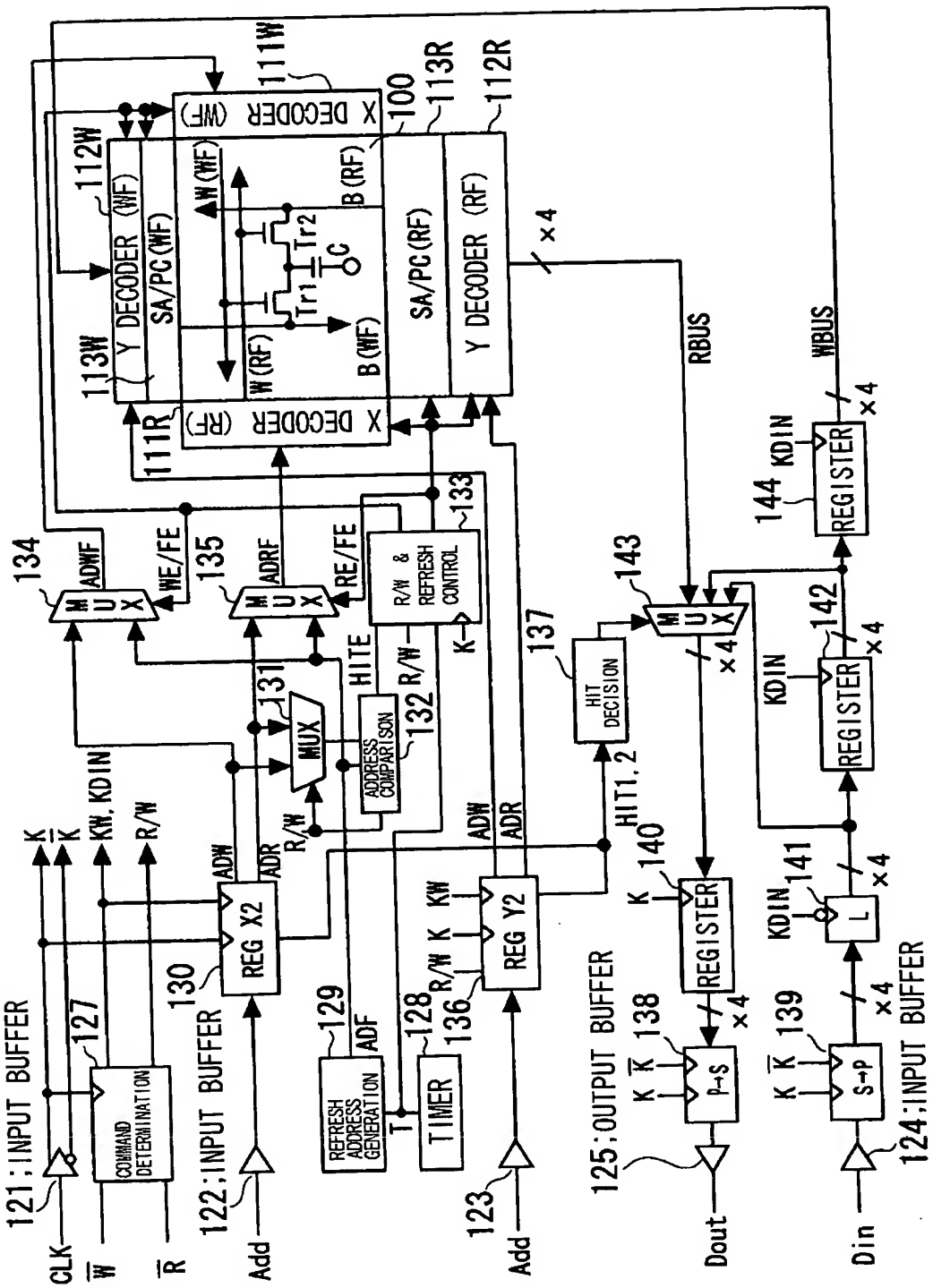
FIG. 1


X DECODER (WF)
111W
100
113R
112R
112W
Y DECODER (WF)
SA/PC(WF)
W(WF)
B(RF)
Tr2
Tr1
C
W(RF)
B(WF)
SA/PC(RF)
Y DECODER (RF)
×4
X DECODER (RF)
111R
113W
RBUS
WBUS
134
ADWF
WE/FE
135
ADRF
RE/FE
R/W & REFRESH CONTROL
133
144
KDIN
REGISTER
×4
143
137
HIT DECISION
142
HITE
131
MUX
132
ADDRESS COMPARISON
R/W
K
ADW
ADR
HIT1, 2
140
K
REGISTER
×4
KDIN
141
L
×4
121;INPUT BUFFER
CLK
W
R
127
COMMAND DETERMINATION
130
REG X2
122;INPUT BUFFER
Add
129
ADF
REFRESH ADDRESS GENERATION
128
TIMER
136
R/W K KW
REG Y2
123
Add
125;OUTPUT BUFFER
K K 138
P→S
×4
Dout
K K 139
S→P
×4
Din
124;INPUT BUFFER
KW, KDIN
R/W

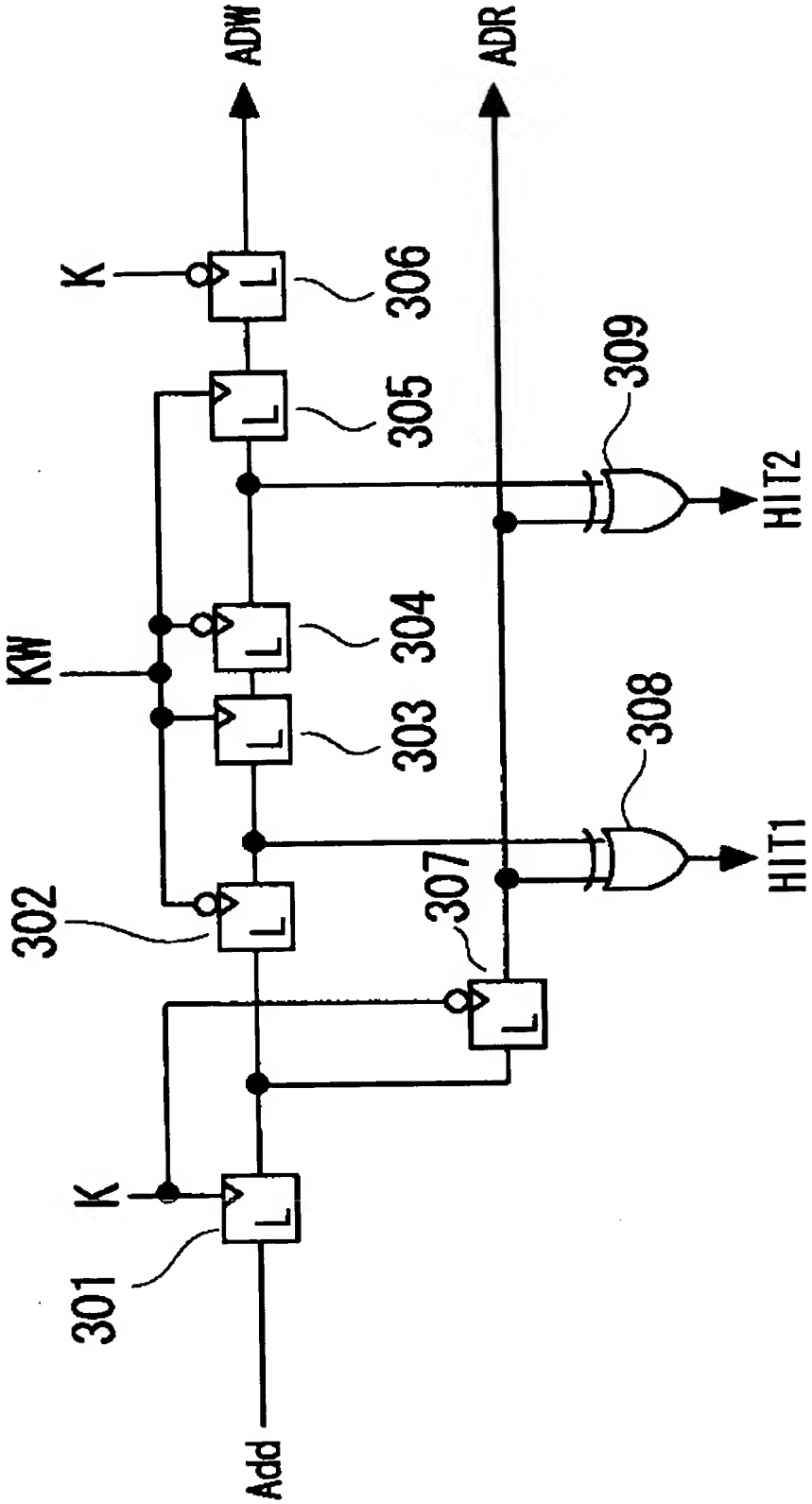
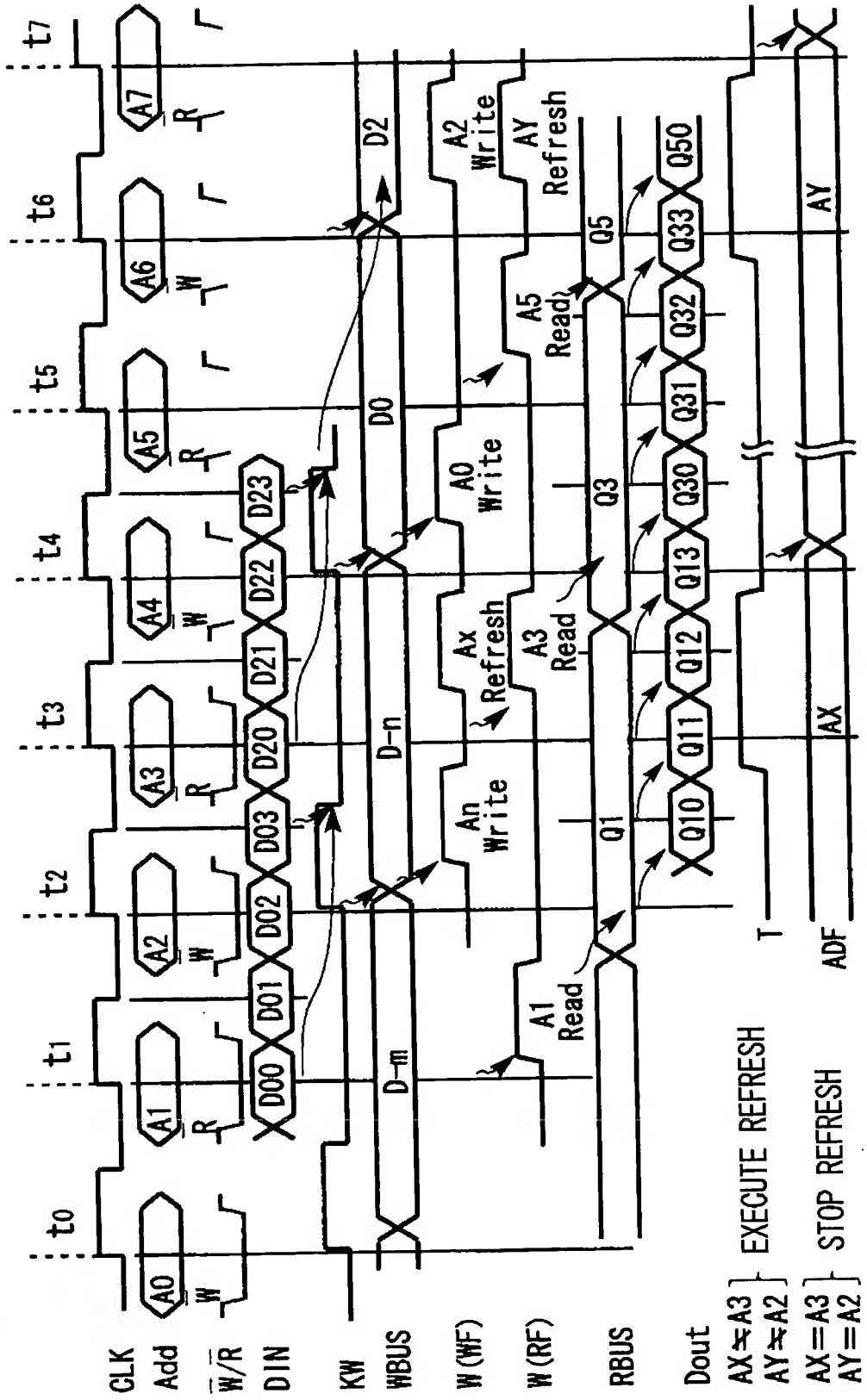


FIG. 2

FIG. 3


t0
t1
t2
t3
t4
t5
t6
t7
CLK
Add
W/R
DIN
KW
WBUS
W (WF)
W (RF)
RBUS
Dout
AX≠A3
AY≠A2
AX=A3
AY=A2
EXECUTE REFRESH
STOP REFRESH
T
ADF
A0
A1
A2
A3
A4
A5
A6
A7
D00
D01
D02
D03
D20
D21
D22
D23
D-m
D-n
D0
D2
An Write
Ax Refresh
A0 Write
A2 Write
A1 Read
A3 Read
A5 Read
AY Refresh
Q1
Q3
Q5
Q10
Q11
Q12
Q13
Q30
Q31
Q32
Q33
Q50
AX
AY

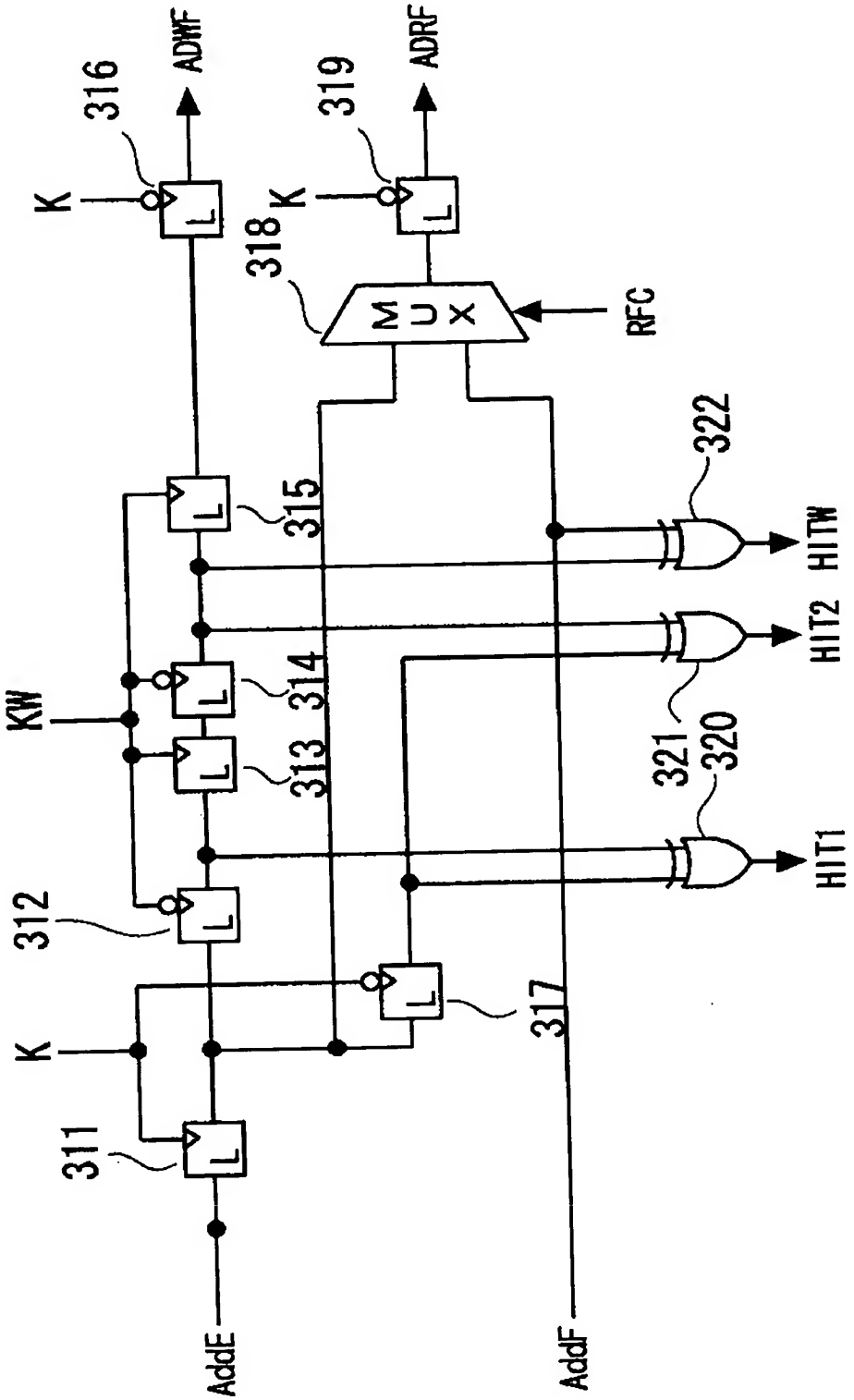

316
ADWF
319
ADRF
K
K
318
MUX
RFC
322
315
HITW
HIT2
KW
314
313
321
320
HIT1
312
K
317
311
AddE
AddF

FIG. 4

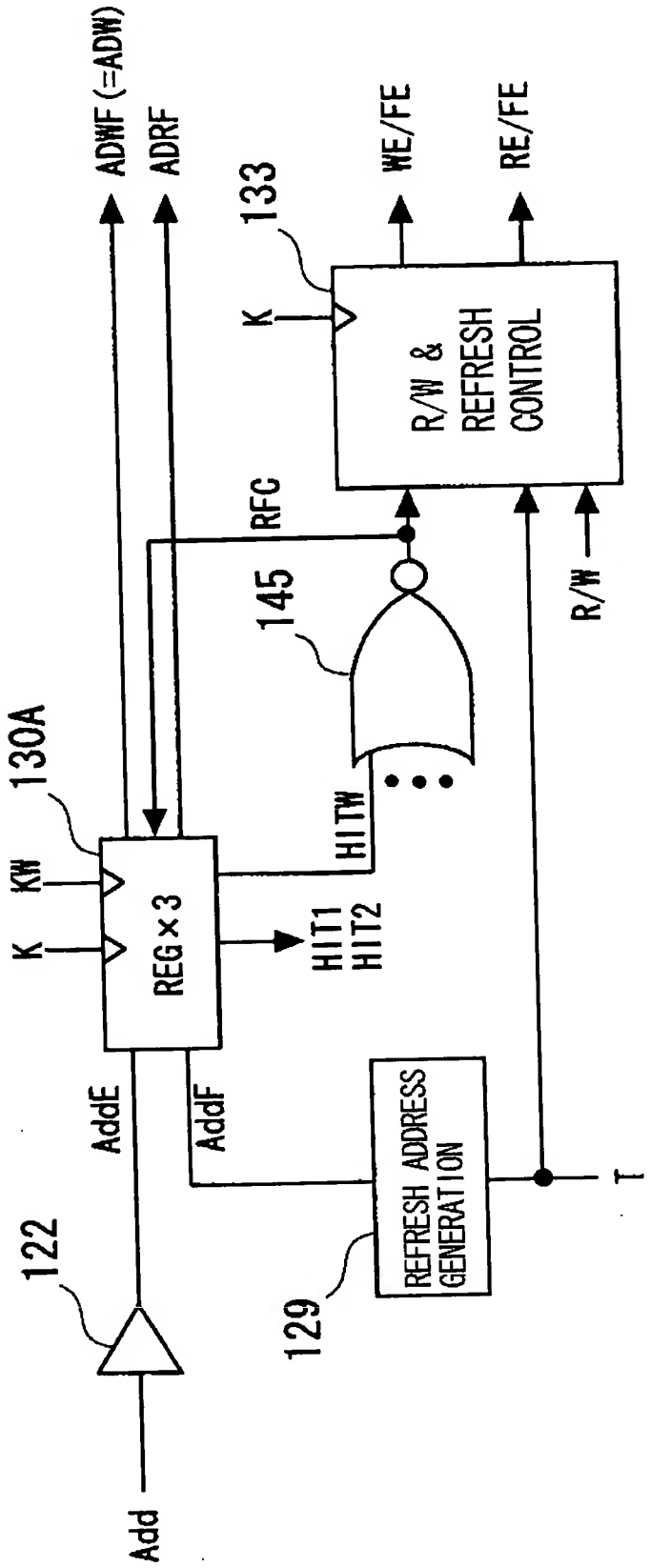

ADWF (=ADW)
ADRF
WE/FE
RE/FE
133
K
R/W &
REFRESH
CONTROL
RFC
145
R/W
130A
KW
K
REG×3
HITW
HIT1
HIT2
AddE
AddF
REFRESH ADDRESS
GENERATION
T
122
129
Add

FIG. 5

FIG. 6

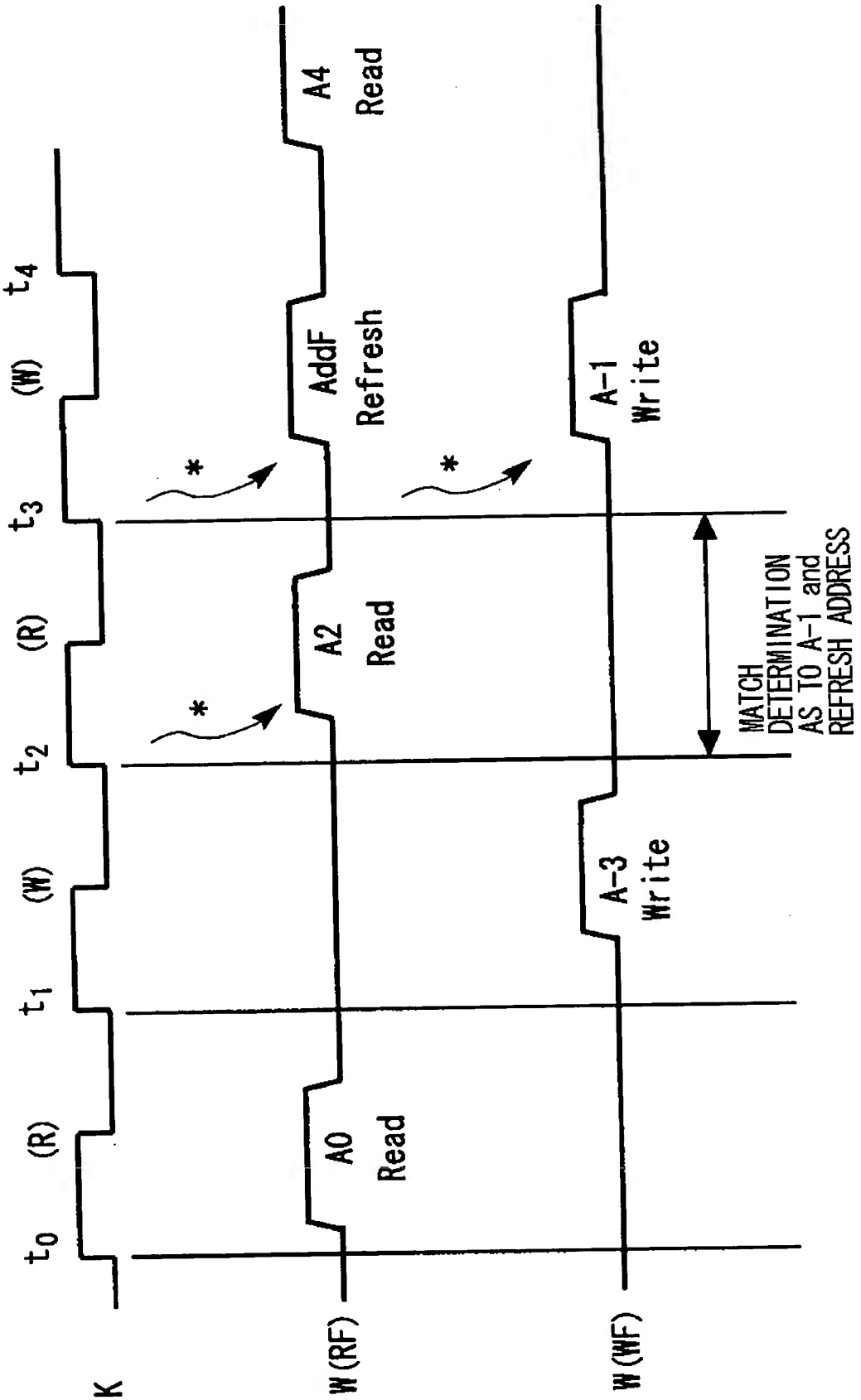

t0
(R)
t1
(W)
t2
(R)
t3
(W)
t4
K
W(RF)
W(WF)
A0
Read
A2
Read
AddF
Refresh
A4
Read
A-3
Write
A-1
Write
*
*
*
MATCH
DETERMINATION
AS TO A-1 and
REFRESH ADDRESS

FIG. 7

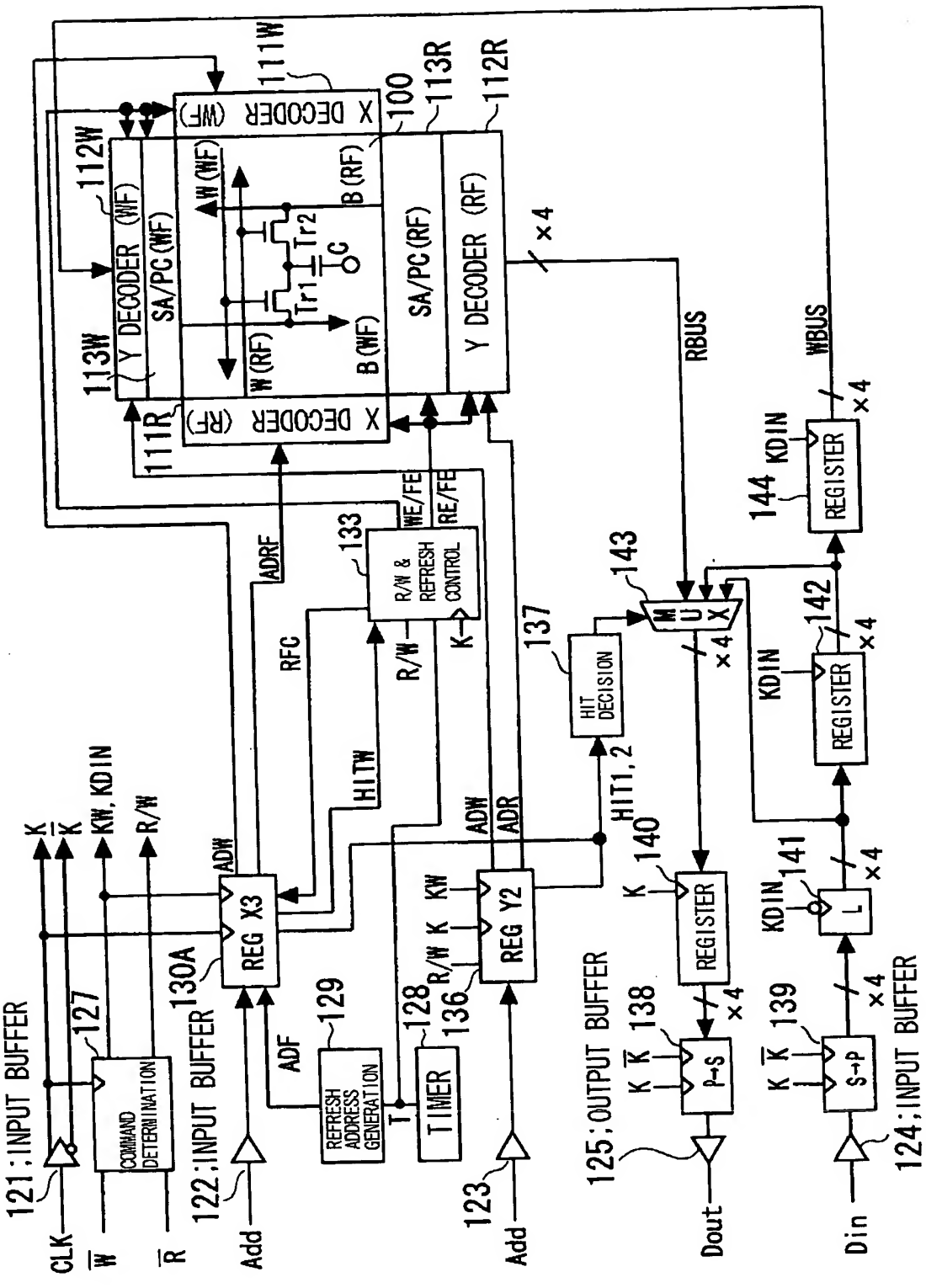
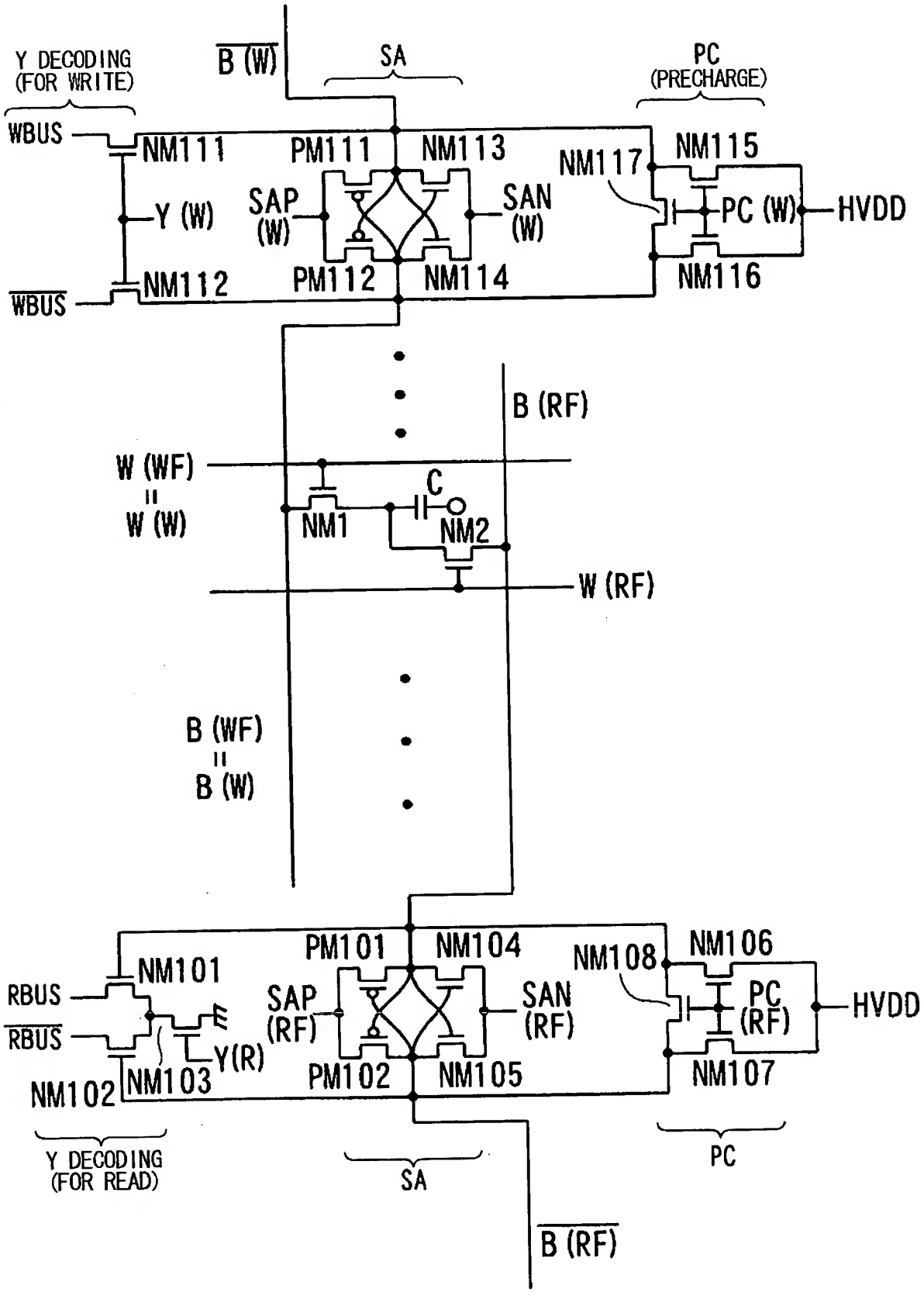

X DECODER (WF)
111W
100
113R
112R
112W
Y DECODER (WF)
SA/PC (WF)
W (WF)
B (RF)
Tr1
Tr2
C
W (RF)
B (WF)
SA/PC (RF)
Y DECODER (RF)
×4
113W
X DECODER (RF)
111R
RBUS
WBUS
WE/FE
RE/FE
133
R/W & REFRESH CONTROL
ADRF
RFC
R/W
K
HITW
ADW
ADR
137
HIT DECISION
HIT1, 2
143
M U X
×4
144
KDIN
REGISTER
×4
142
KDIN
REGISTER
×4
140
K
REGISTER
×4
141
KDIN
L
×4
K K̄ 138
P→S
×4
K K̄ 139
S→P
×4
121; INPUT BUFFER
127
COMMAND DETERMINATION
CLK
W̄
R̄
K
K̄
KW, KDIN
R/W
122; INPUT BUFFER
130A
REG X3
ADW
Add
ADF
129
REFRESH ADDRESS GENERATION
T
128
TIMER
136
R/W K KW
REG Y2
ADW
ADR
123
Add
125; OUTPUT BUFFER
Dout
124; INPUT BUFFER
Din

FIG . 8


Y DECODING (FOR WRITE)
B (W)
SA
PC (PRECHARGE)
WBUS
NM111
PM111
NM113
NM117
NM115
Y (W)
SAP (W)
SAN (W)
PC (W)
HVDD
WBUS
NM112
PM112
NM114
NM116
B (RF)
W (WF) = W (W)
C
NM1
NM2
W (RF)
B (WF) = B (W)
PM101
NM104
NM108
NM106
NM101
RBUS
RBUS
SAP (RF)
SAN (RF)
PC (RF)
HVDD
Y(R)
NM102
NM103
PM102
NM105
NM107
Y DECODING (FOR READ)
SA
PC
B (RF)

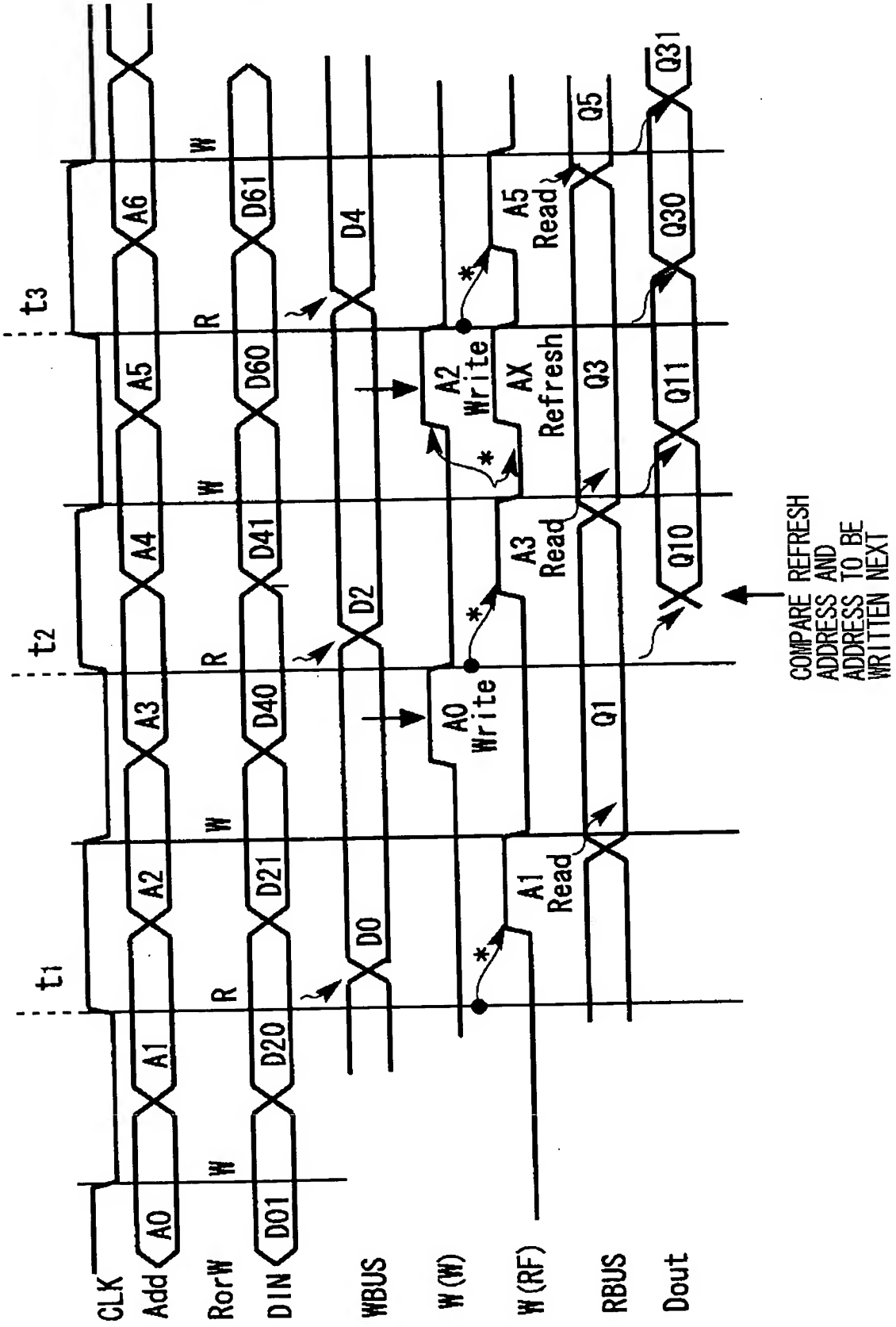

CLK
Add
RorW
DIN
WBUS
W(W)
W(RF)
RBUS
Dout
t1
t2
t3
A0
A1
A2
A3
A4
A5
A6
D01
D20
D21
D40
D41
D60
D61
D0
D2
D4
A0 Write
A1 Read
A2 Write
A3 Read
AX Refresh
A5 Read
Q1
Q3
Q5
Q10
Q11
Q30
Q31
COMPARE REFRESH ADDRESS AND ADDRESS TO BE WRITTEN NEXT

FIG. 9

FIG. 10

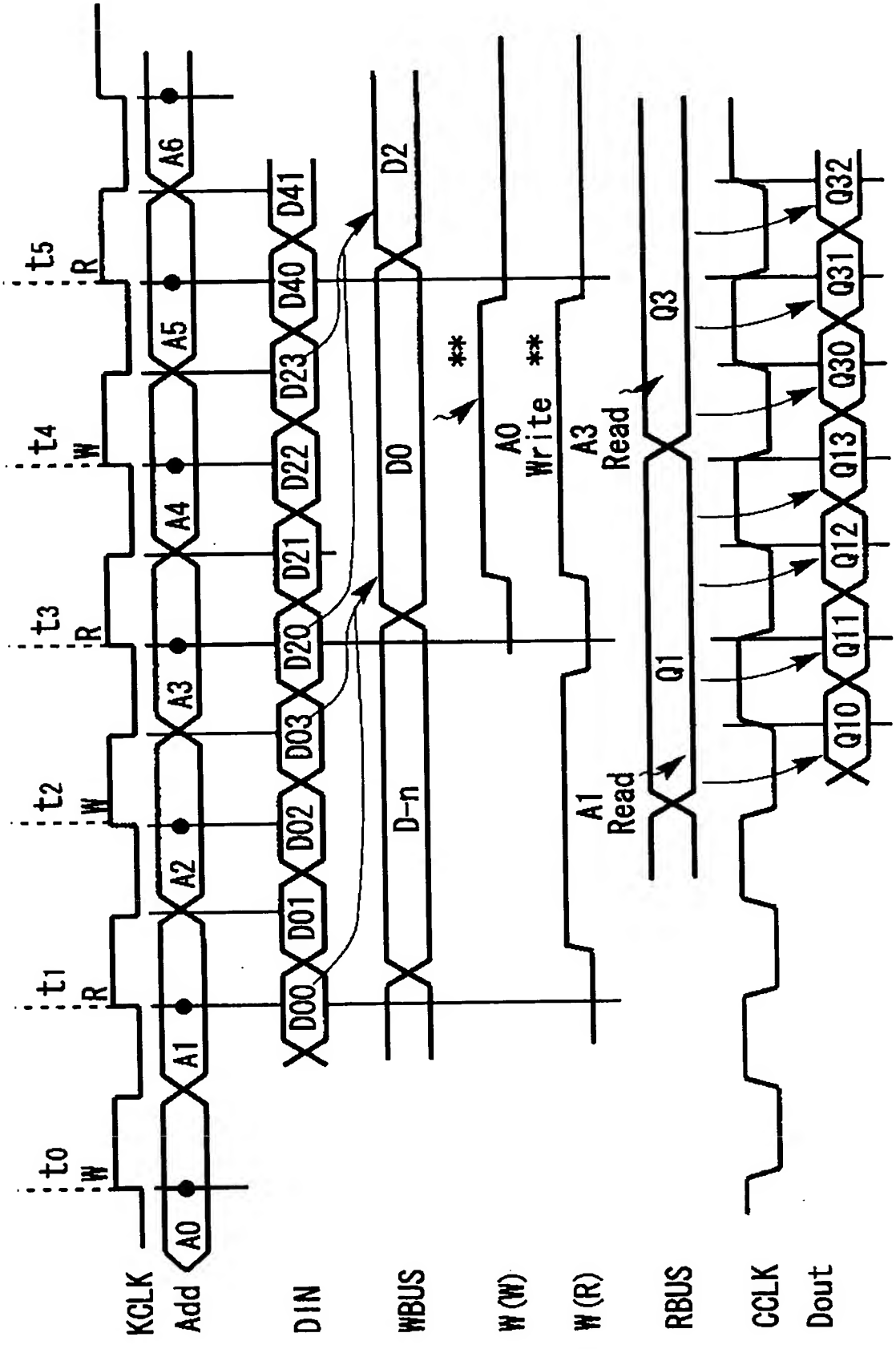

KCLK
Add
DIN
WBUS
W(W)
W(R)
RBUS
CCLK
Dout
t0
t1
t2
t3
t4
t5
W
R
A0
A1
A2
A3
A4
A5
A6
D00
D01
D02
D03
D20
D21
D22
D23
D40
D41
D-n
D0
D2
A0 Write
A3 Read
A1 Read
**
Q1
Q3
Q10
Q11
Q12
Q13
Q30
Q31
Q32

FIG. 11

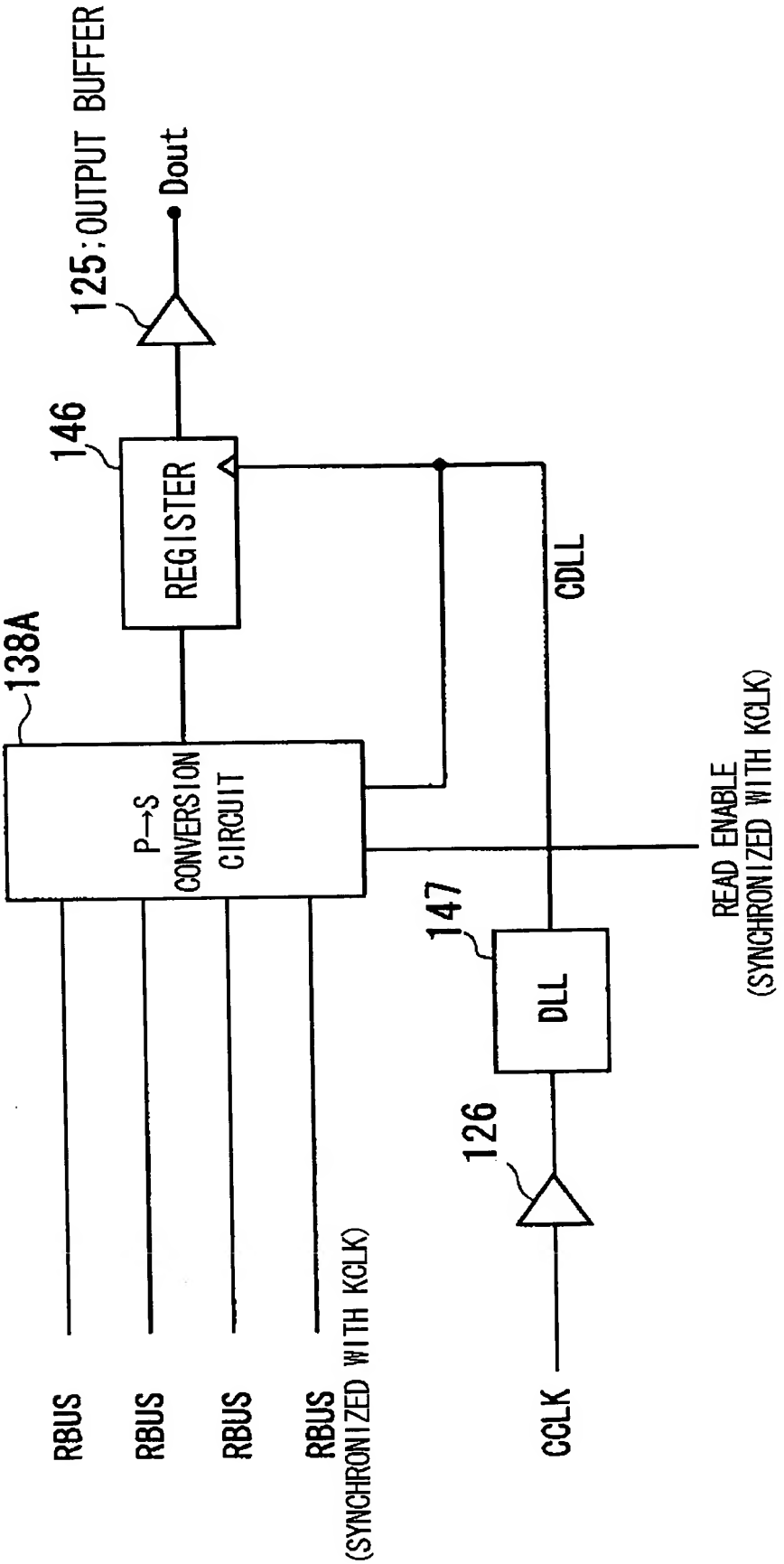

125: OUTPUT BUFFER
Dout
146
REGISTER
CDLL
138A
P→S CONVERSION CIRCUIT
READ ENABLE (SYNCHRONIZED WITH KCLK)
147
DLL
126
RBUS
RBUS
RBUS
RBUS (SYNCHRONIZED WITH KCLK)
CCLK

FIG . 12

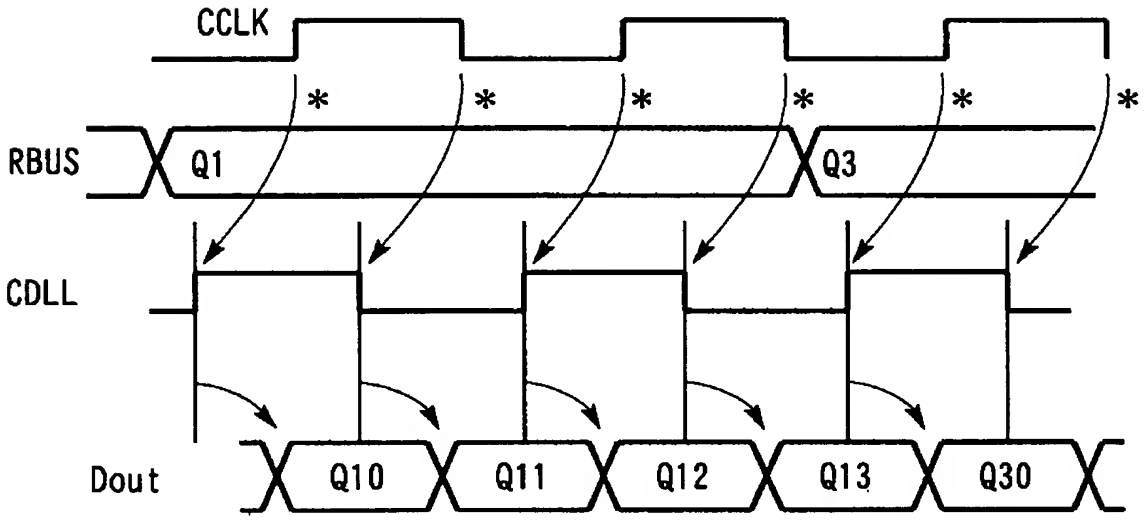


FIG . 13

PRIOR ART